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Printed, Self-Aligned Side-Gate Organic Transistors with a Sub-5 μm Gate–Channel Distance on Imprinted Plastic Substrates

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Printed electronics is an emerging field for the manufacture of electronic devices with low cost and minimal material waste for a wide range of applications, including displays, distributed sensing, smart packaging, and energy management.[1–6] Printing processes are compatible with roll-to-roll production formats and flexible substrates, which are promising for high-throughput manufacturing of flexible electronics.[7,8] Printed thin-film transistors based on solution-processable materials are the fundamental building block of electronic systems and have been the focus of intensive research.[9–15] Despite considerable progress in printed transistors, manufacture using roll-to-roll techniques is still challenging due to the required alignment precision. Layer-to-layer alignment with micrometer-level tolerance is imperative for multilayered devices, but alignment accuracy is hindered by the precision of printing processes as well as control of web speed and tension. To address this issue, self-aligning strategies have been introduced utilizing selective etching, surface energy patterning, and capillary lithography; however, more research is necessary to improve device performance and broaden the range of application.[16–18]

Transistors gated by electrolyte dielectrics have attracted substantial attention for printed electronics because the electrolyte offers excellent compatibility with solution-phase printing techniques and high capacitance, enabling low-voltage operation desirable for low-power and portable devices.[19–23] Such transistors operate by migration of electrolyte ions toward the gate electrode and the semiconductor upon application of a gate voltage. This electrolytic nature of gating enables the transistors to be constructed with a side-gate architecture, allowing simple device structure and easy fabrication.[24–29] Unlike conventional transistor structures with the gate electrode located on top or underneath the semiconductor, the side-gate geometry places the gate electrode next to the transistor on the substrate, resulting in a long gate distance defined as the distance between the gate electrode and the semiconducting channel (between the source and the drain). The long gate distance reduces the electric field created by the gate potential and consequently retards ion transport in the electrolyte,[24] leading to low switching speeds and a sweep rate-dependent transfer characteristic. These unfavorable features in side-gate transistors have so far limited their use in real device applications. Although decreasing the gate distance is expected to improve device speed, the typical printing resolution (e.g., piezoelectric inkjet printing resolution ≥ 20 μm) restricts the gate distance to several tens of micrometers for printed side-gate transistors.

Here we describe a printing strategy to reduce the gate distance considerably and improve the device performance of side-gate transistors using a self-aligning, high-resolution, and scalable process. The processing method, self-aligned capillarity-assisted lithography for electronics (SCALE),[18] is based on capillary action of liquid inks in channels and reservoirs imprinted on plastic substrates. In SCALE, inks are delivered to reservoirs (diameter: hundreds of micrometers) by inkjet printing and transported to channels connected to the reservoirs by capillary flow, allowing self-alignment with generous printing tolerance (≈reservoir size) and high-resolution patterning with the use of submicron capillary channels. Employing the SCALE process, we have achieved printed side-gate transistors with a gate distance of 4.6 μm and characterized their electrical performance.

Figure 1 depicts a schematic diagram for the fabrication of a transistor by the SCALE process (details in the Experimental Section). Capillary channels and reservoirs were first imprinted on a plastic film using a polydimethylsiloxane (PDMS) stamp and UV-curable polymer coating. Prior to imprinting, the PDMS stamp was prepared from a Si master mold where capillary channels and reservoirs were generated by two photolithography cycles for microchannels and reservoirs and focused ion beam (FIB) lithography for nanochannels (Supporting Information, Figure S1). The stamp was used without any modification after fabrication. The bare plastic film was plasma-treated to enhance the adhesion of the coating prior to the application of the UV-curable polymer and pressing by the PDMS stamp (Figure 1a). After curing by UV light, the PDMS stamp was easily peeled off without any damage, and left behind the capillary channels and reservoirs on the polymer coating (Figure 1b). The PDMS stamp can be used repeatedly to make

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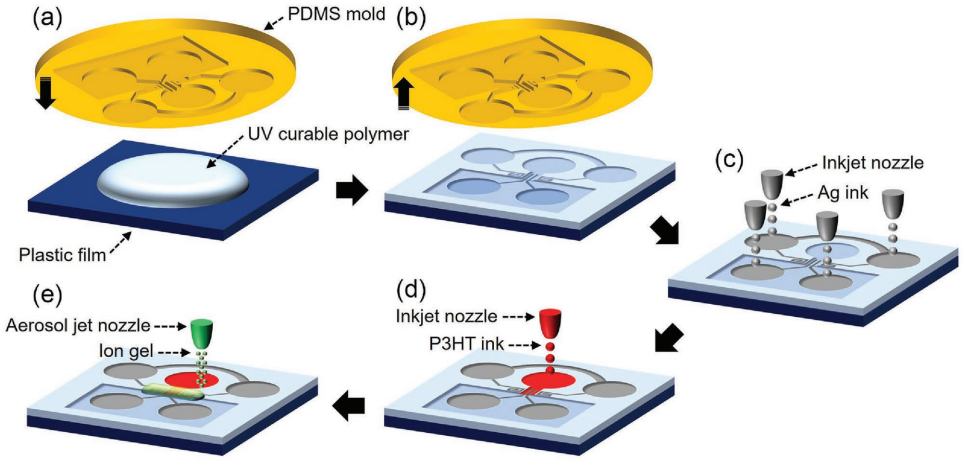

Figure 1. Fabrication steps for a transistor using the SCALE process. a) UV-curable polymer was placed on a plastic film and pressed by a PDMS stamp. b) The stamp was separated from the polymer coating after UV curing. c) A reactive ion Ag ink was inkjet-printed onto the imprinted reservoirs for source, drain, and gate electrodes, followed by Cu electroless plating (not shown). d) A semiconducting P3HT ink was inkjet-printed onto the reservoir connected with the semiconductor channel. e) An ion gel ink was aerosol-jet-printed on the transistor region for the gate dielectric.

more imprinted substrates until it becomes contaminated by the photopolymer or dust particles. To form electrodes (Figure 1c and Supporting Information, Figure S2a), an Ag ink was delivered to source, drain, and gate reservoirs by inkjet printing after plasma treatment of the imprinted substrate to enhance the surface energy and increase the capillary driving force. The sample was then annealed and submerged in a Cu electroless plating bath to develop a thin Cu coating on the printed Ag for more conformal contact of the semiconductor with the source and drain electrodes around the channel edges.[18] For a semiconducting layer (Figure 1d and Supporting Information, Figure S2b), poly(3-hexylthiophene) (P3HT) ink was delivered to the semiconductor reservoir by inkjet printing. Finally, an ion gel gate dielectric was printed to complete the device (Figure 1e and Supporting Information, Figure S2c). The dielectric layer was printed by aerosol jet printing without the use of capillary action, because precise alignment was not necessary for the gate dielectric, which encompassed the whole transistor region.

Figure 2a displays an optical microscopy (OM) image of the reservoirs and capillary channels on the Si master mold. One device contains five reservoirs (diameter and depth: 500 and 5 µm, respectively) to receive inks for the source, drain, gate, and semiconductor. Capillary channels are connected to the reservoirs and designed to deliver the inks to the transistor region (Figure 2b). The gate channels (width and depth: 10 and 5 µm, respectively) are placed close to the semiconductor channel (width and depth: 6 and 2 µm, respectively) with a gap of 1.6 µm. The source and drain channels comprise microchannels (width and depth: 20 and 5 µm, respectively) and nanochannels (width and depth: 500 and 1000 nm, respectively); the microchannels are connected to the reservoirs and serve to deliver the Ag ink to the transistor region, and the nanochannels (Figure 2c) are connected to the termini of the microchannels and extend into the semiconductor channel in the transistor region. The gap between the source and drain nanochannels is 1.5 µm. Channels and reservoirs on the Si master mold were transferred to the plastic substrate by the imprinting process, as shown in Figure 2d. This OM image shows patterns nearly identical to those on the Si mater mold (Figure 2b), revealing excellent reproduction of the patterns by imprinting. In addition, significant differences between dimensions of the patterns on the Si master mold and imprinted substrate were not observed.

To form electrodes, a reactive Ag ink was delivered to source, drain, and gate reservoirs and wicked into the channels via capillarity. The ink traveled to the end of the channels without noticeable overflow out of the channels. This reactive ion Ag ink possesses a low viscosity (10–12 cP) that enables both inkjet printing and excellent channel infilling due to capillary forces. Although the ink is particle free (Supporting Information, Figure S3), it forms Ag nanoparticles upon printing and annealing (Supporting Information, Figure S4).[30] The Ag metal surface is free from significant organic residue, enabling the printed and infilled features to serve as an excellent seed layer for Cu electroless plating. **Figure 3**a shows a scanning electron microscopy (SEM) image of the electrodes after Ag printing and Cu plating. For the gate, the Ag ink traveled to the end of the capillary channels leaving behind a metal layer without a significant variation in thickness. For the source and drain, continuous metal traces were generated in the micro- and nanochannels, further indicating that the ink flowed successfully into the nanochannels after passing through the microchannels. The FIB cross-section (Figure 3b) along the dotted line A presented in Figure 3a shows that the metal layer deposited on both the sidewalls and bottom of the capillary channel, indicating that the ink filled the channel almost to the top during the capillary flow. In addition, the SEM images (Figure 3c and Supporting Information, Figure S5) of the nanochannels reveal successful Ag/Cu metal patterning for the source and drain nanochannels without shorting. The thickness of printed Ag was ≈400 nm in microchannels and ≈50 nm in nanochannels, and the Cu coating thickness was ≈50 nm. To further examine the device geometry, the FIB cross-section along the dotted line B presented in Figure 3a was obtained as shown in Figure 3d, and its corresponding illustration is provided in **Figure 4**a.

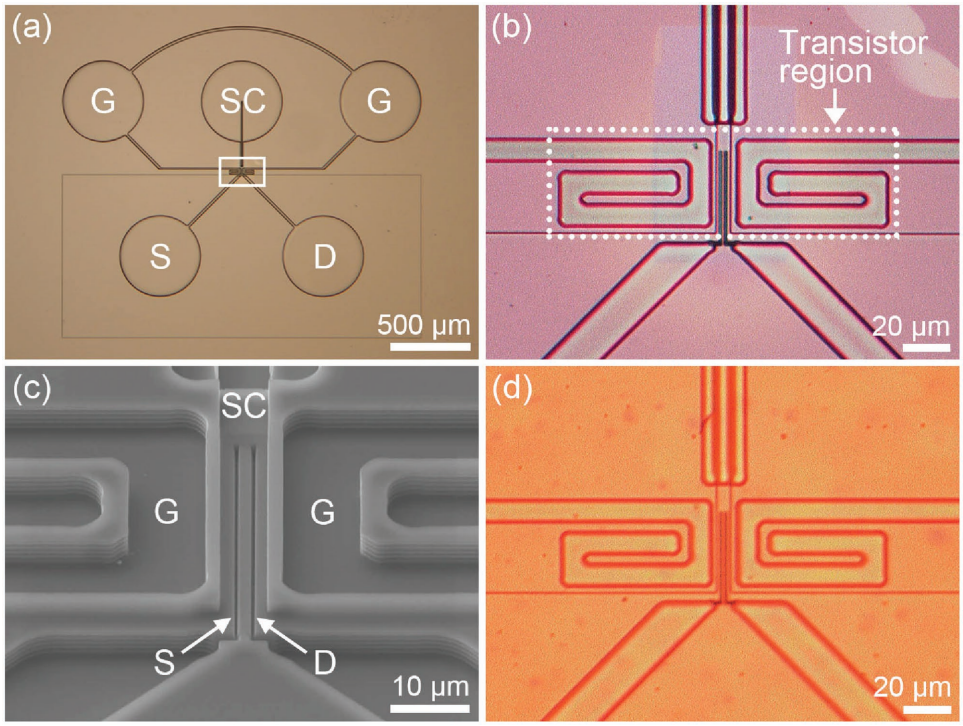

Figure 2. a) Optical microscopy (OM) image of the patterns etched on a Si master mold. One device has five reservoirs for source (S), drain (D), gate (G), and semiconductor (SC). b) Enlarged OM image for the box in part (a). The dotted box in the figure indicates the transistor region. c) Tilted SEM image of the capillary channels in the transistor region. d) OM image for the imprinted polymer coating on a plastic film.

Following the formation of the source, drain, and gate electrodes (Figure 4a), a P3HT (p-type semiconducting polymer) ink was printed for the semiconductor channel (Figure 4b). The P3HT ink used was prepared by dissolving the polymer in a high boiling point (BP) solvent, 1,2-dichlorobenzene (BP ≈ 180 °C). This solvent was selected over other common solvents for P3HT like chloroform (BP ≈ 61 °C) and chlorobenzene (BP ≈ 131 °C) because slower solvent evaporation contributes to longer capillary flow due to slower viscosity rise during flow in the open channel.[31] When delivered to the reservoir, the P3HT ink filled the semiconductor channel and coated the source and drain electrodes after solvent evaporation, as shown in the schematic illustration of Figure 4b. Our previous report has shown good smoothness of the P3HT film deposited by capillarity.[18] The transistor region was then covered with the ion gel gate dielectric, as shown in Figure 4c. The ion gel is a solid polymeric electrolyte consisting of a gelling triblock copolymer and an ionic liquid, and provides high capacitance attributable to mobile ions in the polymer matrix. Supporting Information (Figure S6) shows an OM image of the completed device. The device footprint (substrate area per transistor) is about 4 mm^2, which is relatively large considering the size of the transistor region (≈0.006 mm^2). This large footprint is primarily due to the large reservoir size, resulting from the limitation of our inkjet printing system; however, we expect that the reservoir size can be considerably reduced by employing inkjet printheads capable of producing droplets with a diameter less than 10 μm with automated x–y motion control, allowing a decrease of the reservoir size as well as the device footprint.

As shown in the cross-sectional illustration (Supporting Information, Figure S7) of the completed devices, the side-gate transistors could be printed with a short gate distance (4.6 μm) and transistor channel length (gap between the source and drain nanochannels: 1.5 μm) by the SCALE process. Using this process, high-resolution and self-aligned printing can be achieved because the inks remain confined within the channels during capillary flow and are aligned by the channels into predesigned device structures. In addition, the use of the reservoirs for ink delivery enables us to avoid precise printing alignment, indicating a promising method for roll-to-roll manufacturing.

The electrical performance of the fabricated transistors was tested. For this measurement, the metal-coated source, drain, and gate reservoirs served as contact pads for probes. The probe contact for the gate was made with only one of the two gate reservoirs because they were purposefully connected to each other, as shown in the Supporting Information (Figure S6). The resistance per unit length of the interconnection between the two gate reservoirs was measured to be 33 Ω mm^{-1} (Supporting Information, Figure S8). **Figure 5**a,b displays representative transfer and output characteristics of the devices, respectively. The transfer curve acquired at a sweep rate of 50 mV s^{-1} and a drain voltage (V_D) of –1 V revealed good device operation, with a gate voltage (V_G) less than 2 V and minor current hysteresis between forward and backward scans. The output curve shows desirable linear and saturation behavior at low and high drain voltages. Notably, unlike side-gate transistors reported,[25,32] the fabricated devices exhibited negligible change in transfer curves upon accelerating the sweep rate from 50 to 500 mV s^{-1}, as shown in Figure 5c, which is comparable to top-gate devices.[33]

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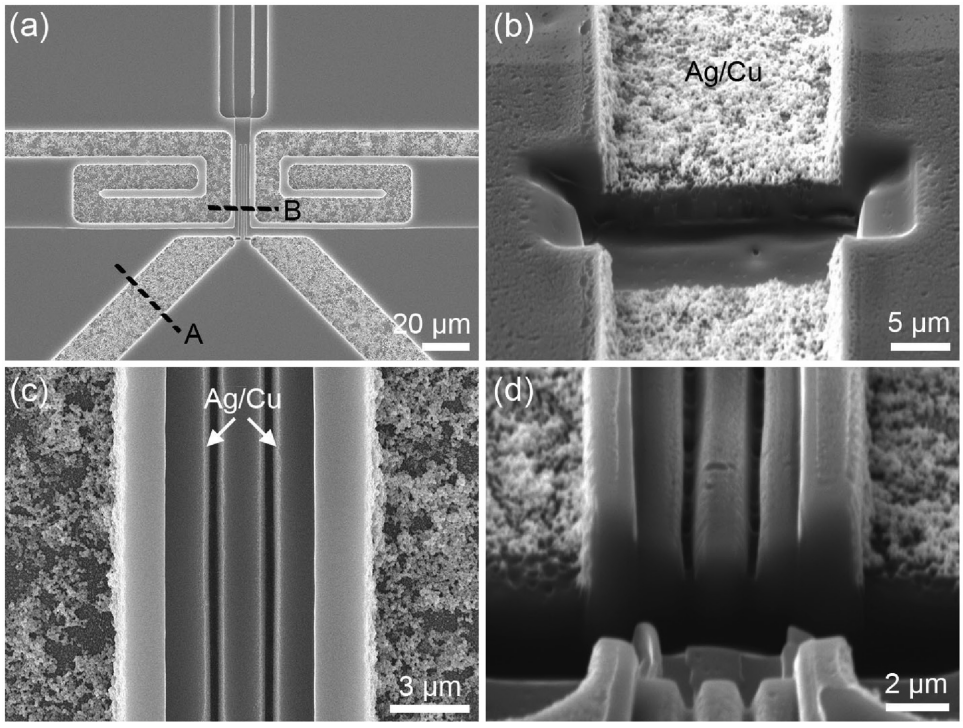

Figure 3. SEM images for the Ag/Cu source, drain, and gate electrodes on the imprinted plastic substrate after Ag printing and Cu plating. a) Top view of the electrodes in the transistor region. b) FIB cross-section along the dotted line A in part (a). c) Top view of the source and drain nanochannels. d) FIB cross-section along the dotted line B in part (a). Small cracks on the polymer coating surface in parts (b) and (d) are damages by the ion beam during FIB etching for the cross-sections.

This negligible change can be attributed to fast response of the electrolyte ions because of the short gate distance. The device metrics in Figure 5 were collected from devices prepared using the semiconducting P3HT ink at a concentration of 4.5 mg mL^{-1} to obtain the optimized P3HT thickness (≈50 nm),[33] a crucial factor for the device performance. In this SCALE process, the semiconductor thickness can be adjusted with the ink concentration. Supporting Information (Figure S9) shows a drain current increase with ink concentration, resulting from the increase of the semiconductor thickness. The higher off-current with thicker semiconductor is due to more O_2 doping during printing in air.[33] Furthermore, increased hysteresis is evident from the device prepared with 6 mg mL^{-1} ink, originating from impeded ion transport in the thicker semiconductor.[33]

To evaluate statistical distributions of device metrics, 50 devices were printed, and 44 of those were functional, indicating 88% yield. Device failure arose mostly from the impediment to capillary action by dust particles on the substrate surface. Hence, improvement of the yield can be expected when processing in a clean room. As shown in Figure 5d,e, the charge carrier mobility (μ) and the threshold voltage (V_{th}) were calculated to be 0.57 ± 0.28 cm^2 V^{-1} s^{-1} and –1.23 ± 0.14 V,

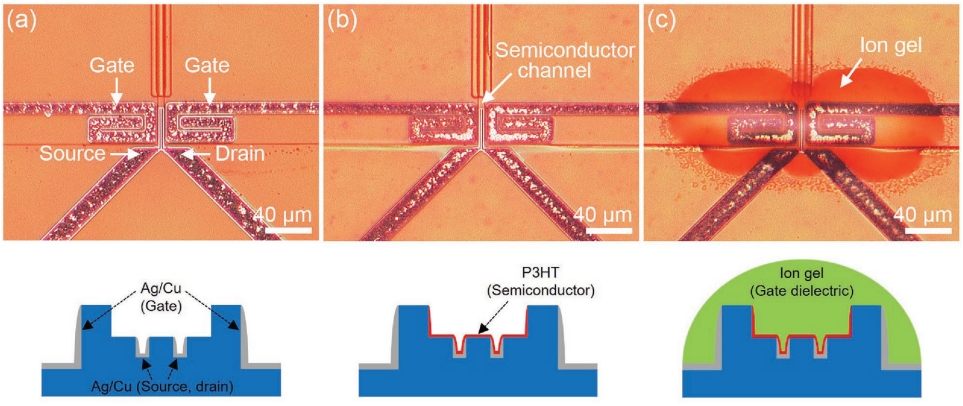

Figure 4. OM images (top) for the device fabrication steps and their corresponding schematic illustrations (bottom) in a cross-sectional view after a) Ag printing and Cu plating for the source, drain, and gate electrodes, b) filling the P3HT ink in the semiconductor channel, and c) printing the ion gel ink for the gate dielectric.

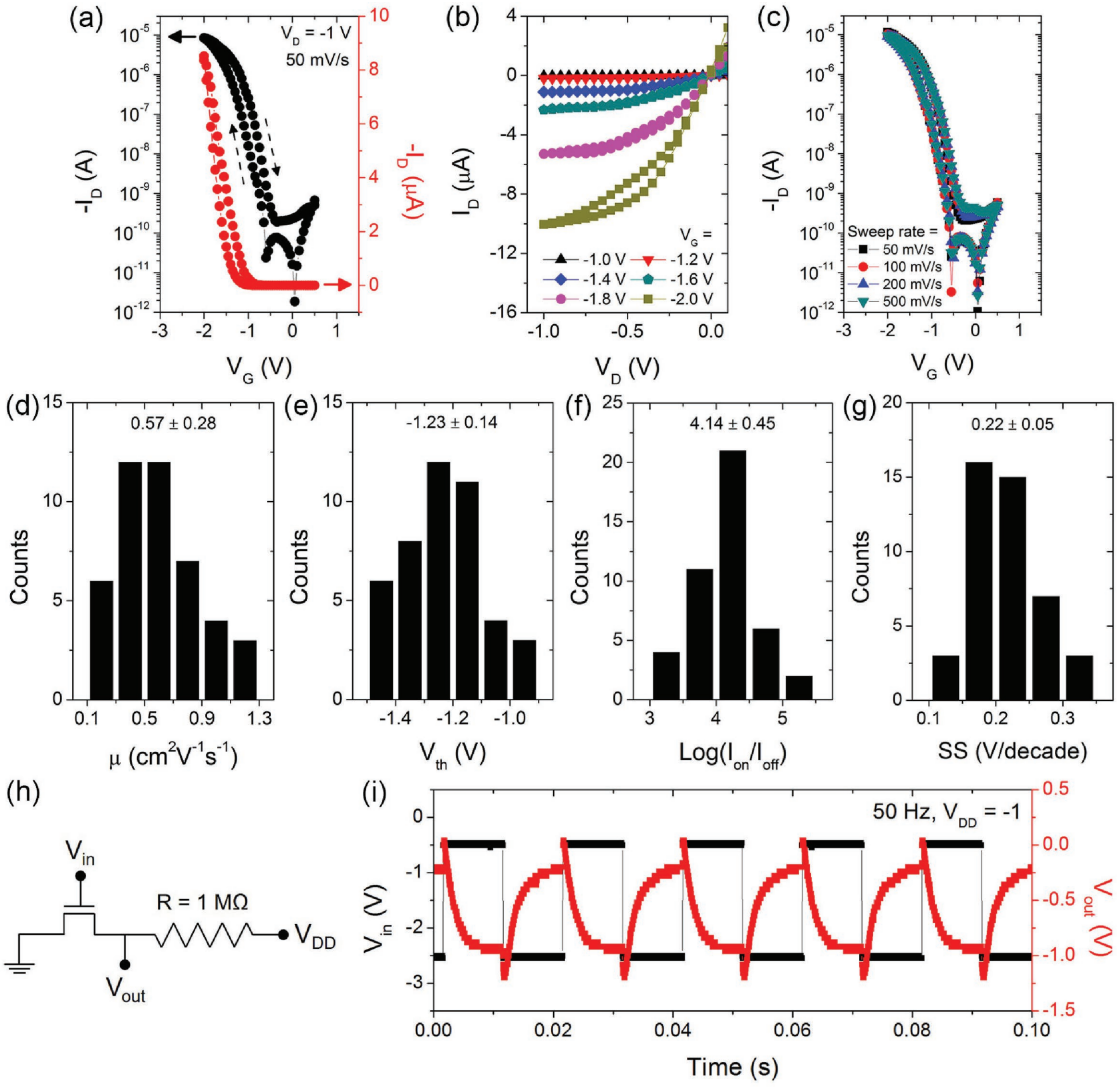

Figure 5. a,b) Representative transfer and output characteristics, respectively, for the fabricated devices. The transfer curve was obtained with a drain voltage (V_D) of –1 V and a gate voltage sweep rate of 50 mV s^{-1}. c) Transfer curves collected as increasing the sweep rates from 50 to 500 mV s^{-1}. d–g) Histograms of device metrics for 44 devices, including the charge carrier mobility (μ), threshold voltage (V_{th}), on/off-current ratio (I_{on}/I_{off}), and subthreshold slope (SS), respectively. h) Schematic diagram and i) dynamic response characteristic of resistor-loaded inverters using the side-gate transistor at a frequency of 50 Hz. The source was grounded and the drain supply voltage (V_{DD}) was –1 V.

respectively, by fitting plots of the square-root drain current ($I_D^{1/2}$) as a function of V_G according to the standard saturation regime relation (Equation (1))

$$I_D = \mu C_i \frac{W}{2L}(V_G - V_{th})^2 \quad (1)$$

The transistor channel width (W) and length (L) are 30 and 1.5 μm, respectively. The specific capacitance (C_i) of the ion gel gate dielectric was estimated to be 2.2 μF cm^{-2} by displacement current measurement (Supporting Information, Figure S10). In addition, the mean on/off-current ratio (I_{on}/I_{off}) was over 10^4, and the subthreshold slope (SS, $dV_G/d(\log I_D)$) was measured to be 0.22 ± 0.05 V per decade, as shown in Figure 5f,g.

For investigation of the switching speed, resistor-loaded inverters were fabricated by connecting the transistor in series with a 1 MΩ resistor, as shown in Figure 5h. Figure 5i displays dynamic performance of the inverters at 50 Hz. Although some output voltage overshooting was observed due to the parasitic capacitance deriving from the high capacitance of the ion gel dielectric,[34] the inverters functioned to convert the low/high input signal to the high/low output signal. The inverters operated with a good output range ($\triangle V_{out}/V_{DD}$, $\triangle V_{out} = V_{out,high} - V_{out,low}$) of 0.8 at operating frequencies from 1 to 50 Hz. Moreover, while the output range decreased, the devices could be switched even at a frequency higher than 100 Hz (Supporting Information, Figure S11). This result is much higher switching speed compared to previously reported inverters using side-gate transistors,[32] indicating the possibility of expanding applications of the side-gate devices.

In summary, we have demonstrated printed side-gate transistors with a gate distance less than 5 μm using a scalable printing

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method referred to as SCALE. The SCALE process facilitated submicron patterning and self-alignment of functional layers without delicate printing control by means of imprint lithography and capillarity of liquid inks on plastic substrates. Consequently, side-gate devices could be fabricated with a short gate distance (4.6 µm) and transistor channel length (1.5 µm), exhibiting desirable transfer and output characteristics without significant sweep rate dependence. Moreover, resistor-loaded inverters employing the transistors were successfully switched at an operation frequency higher than 100 Hz. Overall, our work establishes a scalable printing method for self-aligning and high-resolution patterning of electronically functional inks to advance printed and flexible electronics.

Experimental Section

Si Master Mold Fabrication: An Si master mold was prepared by two photolithography cycles and FIB lithography as described in the Supporting Information (Figure S1). For the first photolithography cycle, an Si wafer was prebaked at 200 °C for 5 min, vapor-coated with hexamethyldisilazane for 3 min, and spin-coated with photoresist (AZ9260) at 300 rpm for 10 s and at 3000 rpm for 60 s, sequentially. After soft-baking at 110 °C for 165 s, the photoresist was exposed to UV light through a predesigned photomask using a mask aligner (MA6, Karl Suss). The wafer was immersed in a developer solution AZ 400K diluted with deionized water (1:4 v/v) for 4 min, and rinsed with deionized water and dried. The features were then etched to a depth of 2 µm by reactive ion etching (SLR-770, Plasma-Therm), and the photoresist was rinsed with acetone, ethanol, isopropanol, and deionized water. The second photolithography cycle was the same with the first cycle, but the etching depth was 5 µm. Finally, nanochannels were generated with a depth of 1000 nm using an FIB system (Quanta 200 3D, FEI).

PDMS Stamp Fabrication: After the Si master mold was silane-treated in a vacuum chamber with 0.2 mL of trichloro(1H,1H, 2H,2H-perfluorooctyl)silane (Aldrich) for 4 h, a mixture of PDMS monomer and its curing agent (10:1 w/w, Sylgard 184, Dow Corning) was poured onto the master mold and cured in an oven at 70 °C for 3 h. The PDMS stamp was peeled off and postcured in an oven at 120 °C for 2 h.

Imprinted Substrate Preparation: A UV-curable polymer (Norland Optical Adhesive (NOA) 73, Norland Products) was coated on a polyimide film (Kapton, Dupont) that was air-plasma-treated (PDC-32G, Harrick Plasma) for 3 min to promote the adhesion of coating. The PDMS stamp was placed onto the coating and the NOA polymer was cured by exposure to UV light (wavelength: 366 nm, UVGL-58, UVP) for 90 min. The stamp was removed from the photopolymer coating following the curing.

Ag Printing and Cu Electroless Plating for Source, Drain, and Gate Electrodes: After air-plasma treatment for 1 min, reactive Ag ink provided by Electroninks was inkjet-printed on the source, drain, and gate reservoirs. The inkjet printing was performed using a custom-built drop-on-demand inkjet printer with an 80 µm diameter nozzle (MJ-AT-01, MicroFab) in air at room temperature. A unipolar waveform was employed consisting of rise, dwell, and fall times of 5, 30, 5 µs, respectively, at a drive voltage and a frequency of 120 V and 1 kHz. After annealing at 100 °C for 5 min, the sample was immersed in a Cu electroless plating bath for 1 min, taken out, rinsed with deionized water, and dried using an air gun. The bath contained 1.4 g of $CuSO_4 \cdot 5H_2O$ (J.T. Baker), 5.1 g of ethylenediaminetetraacetic acid disodium salt (Fisher Scientific), 1.6 g of NaOH (Mallinckrodt), 50 mL of deionized water, and 25 mL of formaldehyde (37% solution, VWR), and was heated on a hot plate at 55 °C during Cu plating.

Printing Semiconductor and Gate Dielectric: A P3HT (Rieke Metals) ink was prepared by dissolving the polymer in 1,2-dichlorobenzene (Sigma-Aldrich) with a concentration of 4.5 mg mL^{-1}, and delivered to the semiconductor reservoir by inkjet printing in air at room temperature. For gate dielectric, an ion gel ink was prepared by mixing triblock copolymer of poly(styrene-b-methylmethacrylate-b-styrene), ionic liquid 1-ethyl-3-methylimidazolium bis(trifluoromethylsulfonyl)imide (EMD Chemicals), and ethyl acetate in a ratio of 1:9:90 (w/w/w). The ion gel ink was deposited using an aerosol jet printer (AJ 200, Optomec) with a 200 µm diameter nozzle, at flow rates of carrier gas and sheath gas of 20 and 40 sccm, respectively. Printing was carried out in air with the substrate temperature maintained at 60 °C to enhance ink drying.

Electrical Measurement: For the transistor characterization, after annealing the fabricated devices at 120 °C for 30 min in a nitrogen glovebox to avoid oxidation of Cu, transfer and output characteristics were measured using a source meter (237, Keithley) and an electrometer (6517A, Keithley) at room temperature. For the inverter characterization, the dynamic measurement was performed with an electrometer (6517A, Keithley) to keep the source grounded and V_{DD} terminal at –1 V, a waveform generator (33500B, Agilent) to create the input square wave signal, and a digital oscilloscope (TDS1002B, Tektronix) to acquire the output response signal. All electrical measurements were carried out in a nitrogen glovebox.

Supporting Information

Supporting Information is available from the Wiley Online Library or from the author.

Acknowledgements

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