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A Self-Aligned Strategy for Printed Electronics: Exploiting Capillary Flow on Microstructured Plastic Surfaces

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Printing is a promising route for high-throughput processing of electronic devices on large-area, flexible substrates by virtue of its integration into roll-to-roll production formats. However, multilayered electronic devices require materials registration with micrometer-level tolerances, which is a serious challenge for continuous manufacturing. Here, a novel, self-aligned manufacturing approach is introduced that allows precision patterning of multilayered electronic devices by inkjet printing on microimprinted plastic substrates. Materials registration is achieved automatically by sequential deposition of liquid inks into multilevel trench networks on the substrate surface using capillary forces. By creating suitable multitier capillary networks, fully self-aligned fabrication of all the major building blocks of an integrated circuit, including resistors, capacitors, transistors, and crossovers, with excellent yields and performance metrics is demonstrated. The current status of inkjet and imprint technologies suggests that this self-aligned manufacturing strategy can be scaled up to large-area substrates with integration densities greater than 1000 devices cm^{-2}.

1. Introduction

Printed electronics is emerging as a low-cost means for integrating electronic devices into flexible, large-area formats for applications including displays,[1,2] identification tagging,[3,4] distributed sensing,[5] and energy harvesting.[6,7] Printing electronically active inks on flexible substrates, such as plastic or paper, is especially attractive because it can be integrated with roll-to-roll (R2R) manufacturing resulting in high-throughput device fabrication. However, it is a challenge to create multilayered devices with the required control over ink placement and feature size. The precise alignment capabilities of photolithography-based semiconductor fabrication do not readily translate to R2R manufacturing, making alignment of multiple layers of disparate materials with micrometer-level tolerances quite difficult to achieve on fast moving webs.

To overcome these challenges, self-aligning strategies are needed that enable materials registration to be achieved automatically during R2R processes. One such strategy is self-aligned imprint lithography (SAIL),[8–10] where all the all key materials are coated onto a web substrate and then a top coat resist is applied. The resist is imprinted with a stamp encoded with geometrical information such that subsequent etching steps selectively reveal specific underlayers (metal, semiconductor, and dielectric) across the substrate. A major drawback of SAIL, however, is that it is a subtractive process, i.e., valuable materials are etched away. Self-aligned inkjet-printed patterns have also been obtained either by confinement of ink droplets in a "bank"[11] or by dewetting on chemically patterned surfaces.[12–15] However, these processes are only partially self-aligned because they require micrometer-level registration of the inkjet nozzle to previously patterned features. Moreover, only a few selective layers of the device stack can be patterned using these techniques, not the entire device.

Here, we report a new approach for printing multilayered electronic devices that is simultaneously self-aligned, additive, and scalable, which relies on capillary flow of electronically active inks within microchannels carefully engineered on the substrate surface. We term this process self-aligned capillarity-assisted lithography for electronics (SCALE). In SCALE, multitier channels, each of which is connected to a separate reservoir, are molded into a coated thermoset material by imprint lithography. The dimensions of the channels range from a few micrometers to tens of micrometers and they are connected to larger reservoirs. Electronic inks are delivered to these reservoirs by "drop-on-demand" inkjet printing from which the liquid inks are wicked into the microchannels by capillarity. The process is self-aligned because multiple inks can be delivered sequentially to cavities engineered into a multilevel microchannel network to form, upon drying, multilayered electronic devices. Importantly, control over the printing process is only required at the size scale of the reservoir (≈hundreds of micrometers) rather than the size scale of the device. Specifically, we demonstrate that all the major multilayered electronic components of an integrated circuit, i.e., resistors, capacitors, transistors, and crossovers can be fabricated using the SCALE process.

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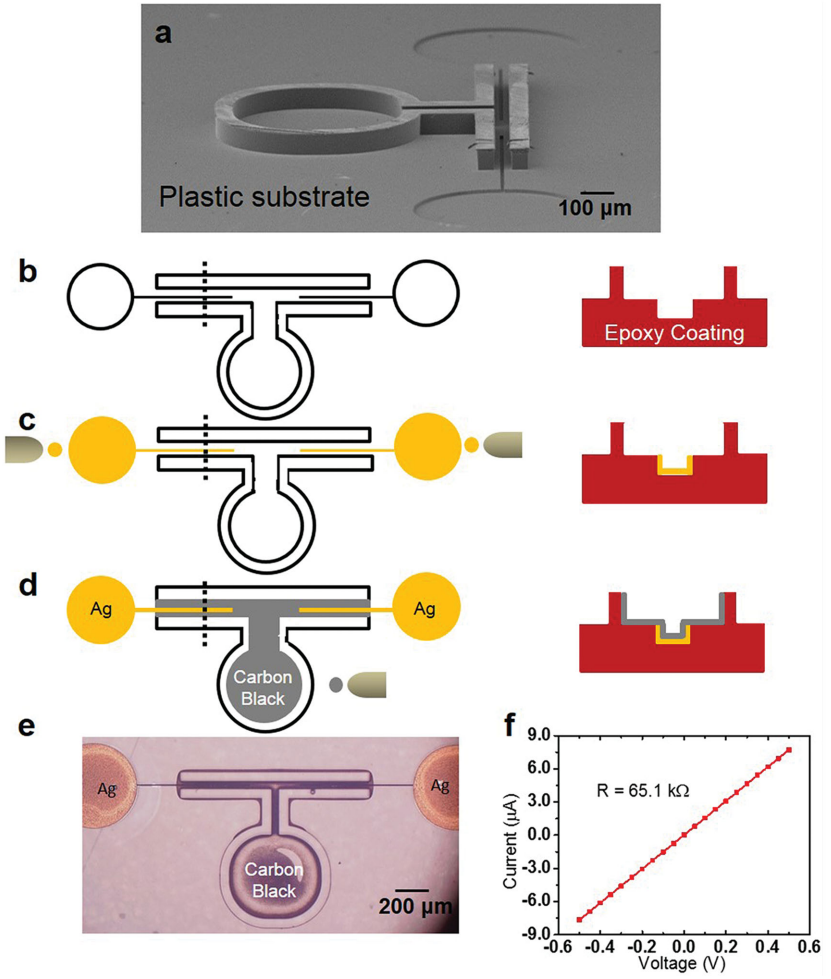

Figure 1. Fabrication of resistors using the SCALE process and electrical characterization. a) SEM image displaying an imprinted device cavity on the surface of an epoxy/PET substrate for processing a resistor. b) Schematic of plan view of the device (left) and cross section along the dotted line (right). c) Metal electrodes are processed by inkjet printing an Ag ink into the yellow reservoirs. The ink is wicked into the channels by capillarity; a thin Ag film is left behind on the channel walls upon annealing (right). d) A carbon black ink is dispensed into the gray reservoir which wicks into the attached channel connecting the two metal electrodes in the process. e) Optical image of a completed device. f) Current–voltage characteristics of the printed device.

2. Results and Discussion

Figure 1 illustrates SCALE fabrication of a single resistor. In the first step, a two-level topographical pattern is created on the surface of a plastic substrate by pressing a polydimethylsiloxane (PDMS) stamp into a liquid epoxy prepolymer coated on a polyethylene terephthalate (PET) film, with subsequent UV curing to solidify the liquid layer (see the Experimental Section). The imprinted features, both recessed and raised, with respect to the substrate surface are shown in the scanning electron microscope (SEM) image in Figure 1a. A schematic of the plan view of the imprinted cavity and the cross section along the dotted line are shown in Figure 1b. A reactive Ag ink[16] is delivered (volume ≈2 nL) to the two lower-level reservoirs by an inkjet nozzle (Figure 1c). Capillarity spontaneously draws this low-viscosity ink (10–12 cP) into the feeder channels (width, w = 10 μm) and fills the cavities.[17–19] The Ag ink is then dried and sintered at 100 °C for 5 min, leaving behind a thin trace of Ag metal on the sidewalls and bottom of the channel and the reservoir. The Ag-coated channels and reservoirs serve as electrodes and electrode pads, respectively. Next, a carbon black ink is loaded into the upper-level reservoir (Figure 1d). This reservoir is connected to a main channel (w = 50 μm) which, in turn, branches into two channels. Again, capillarity drives the ink down the main channel before the flow splits along the two branches, proceeding on top of the two Ag-filled channels. Upon evaporation of the ink solvent, a thin deposit of carbon black is left behind which bridges the two Ag electrodes, completing the resistor fabrication. An optical microscope image of the completed device is shown in Figure 1e. Figure 1f displays the current–voltage characteristics of a typical device, and the nice linear response suggests Ohmic contact between the printed carbon black and Ag films. We fabricated 25 resistors in a single batch and the average value of resistance was measured to be 64.0 ± 2.7 kΩ (see Figure S1 in the Supporting Information). The yield was 100% and the spread in the resistance values was small, indicating excellent reproducibility of the printed layers in all the devices.

To fabricate capacitors using the SCALE process, we adopted an interdigitated architecture, where Ag metal and an "ion gel"[20] polymer electrolyte serve as electrodes and dielectric material, respectively. Ion gels are formed by the gelation of a triblock copolymer (polystyrene-*b*-poly(methylmethacrylate)-*b*-poly(styrene) (PS-PMMA-PS) in an ionic liquid (1-ethyl-3-methylimidazolium bis(trifluoromethylsulfonyl)amide) [EMIM][TFSA]. Ion gel films exhibit very high capacitance values, courtesy of the mobile ions in the polymer matrix, which, upon application of a voltage across the two electrodes, form nanometer-thick electrical double layer (EDL) capacitors at the electrode–electrolyte interfaces.[21] For preparing an inkjet-printable ion gel ink, PS-PMMA-PS and [EMIM][TFSA] (20:80 wt ratio) are codissolved in *n*-butyl acetate, a high boiling solvent to overcome the problem of nozzle clogging during printing (see the Experimental Section).

Similar to the two-tier structure for resistors, cavities at two different elevations are imprinted into the plastic substrate for fabricating capacitors (**Figure 2**a). The lower- and upper-level cavities consist of reservoirs and channels for patterning the Ag electrodes and the ion gel dielectric, respectively. The width and separation of the Ag channels is 10 μm each. In the first of the two printing steps, Ag ink is loaded into the two lower-level reservoirs, which then spontaneously fills the multibranched

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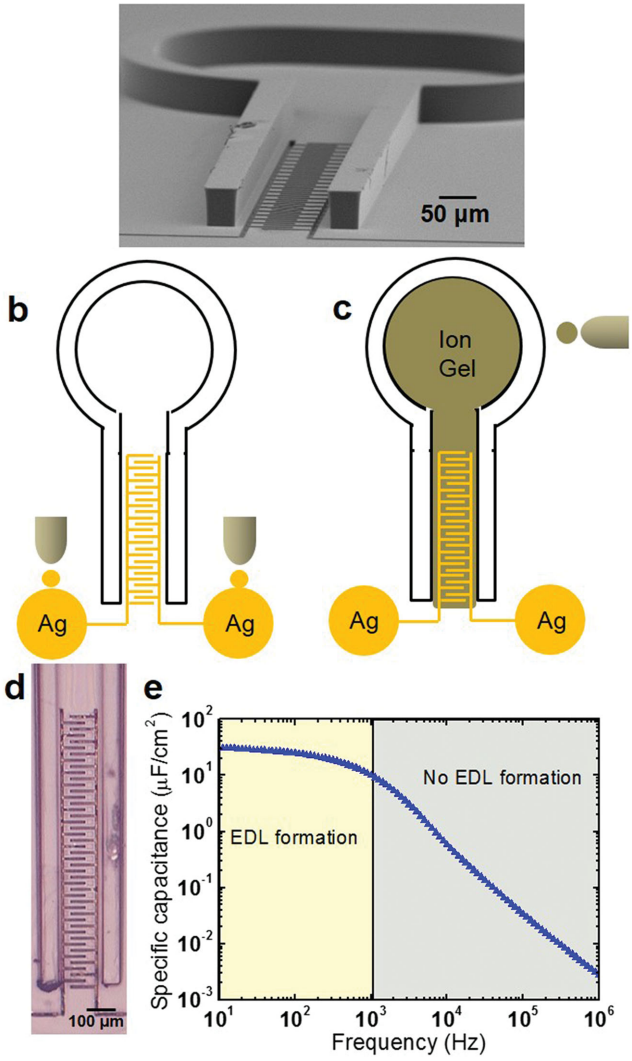

Figure 2. Fabrication of capacitors using the SCALE process and electrical characterization. a) SEM image displaying an imprinted device cavity on the surface of the epoxy/PET substrate for processing a capacitor. Scheme showing fabrication of capacitors by sequential delivery of b) Ag ink to the yellow reservoirs, and c) ion gel ink to the gray reservoir. Both the inks are wicked into their respective channels to form, upon drying and annealing, a self-aligned interdigitated capacitor. d) Optical image of a completed device. e) Frequency dependence of the specific capacitance of the printed capacitors. The capacitance–frequency curve can be divided into two regimes: EDL formation at the Ag–gel interface and no EDL formation.

channels by capillarity (Figure 2b). Upon drying and annealing of the ink, well-defined Ag interdigitated electrodes are obtained with line width comparable to the initial channel width (see Figure S2a in the Supporting Information). In the second printing step, ion gel ink is delivered to the upper-level reservoir, and again, the ink travels down the channel via capillarity, swamping the underlying interdigitated Ag electrodes (Figure 2c). Upon solvent evaporation, which occurs spontaneously without requiring an additional annealing step, an ion gel film is produced between the interdigitated electrodes. An optical image of a portion of the completed device is shown in Figure 2d. Figure 2e shows specific capacitance of the device as a function of frequency from 10 Hz to 1 MHz. A remarkably large capacitance value of about 25 µF cm^{-2} is obtained at 10 Hz, owing to EDL formation at the Ag–gel interfaces. The capacitance value decreases gradually with increasing frequency but remains above 10 µF cm^{-2} even at 1 kHz. At frequencies greater than 1 kHz, the decrease is more dramatic because EDL formation is suppressed. Frequency response of our capacitors strongly depends on the polarization response time of the gel, which may be further improved by decreasing the spacing between the Ag digits. We note that the absolute value of capacitance of the devices can be modulated solely by varying the Ag digit count, with a 1.5 nF capacitance change for every Ag digit (see Figure S2b in the Supporting Information).

To create transistors, which are the most important and complex building blocks of an electronic circuit, by the SCALE process, we adopted electrolyte-gated transistor (EGT) technology,[21] i.e., an electrolyte (ion gel in our case) was employed as the gate dielectric material in the thin film transistor (TFT) stack. EGTs have several key benefits, including low-voltage operation despite relatively high dielectric thickness (≈µm), and the option to physically offset the gate electrode from the source–drain channel.

Given the multiplicity of functional layers in a transistor, a four-tier imprint is created in the plastic substrate. A schematic of the plan view of the device and the cross section along the dotted line is shown in **Figure 3**a. The SEM image in **Figure 4**c displays the complex, high-resolution imprinted device cavity. First, the source and drain electrodes are processed. Ag ink is delivered to the two lowest-lying reservoirs (colored yellow in Figure 3a). As before, Ag-coated channels (w = 5 µm) are obtained after capillary-filling, drying, and sintering of the Ag ink. The printed Ag metal is then coated by a thin film of Cu by immersion in a Cu electroless plating solution for 3 min, followed by a rinse with deionized (DI) water. The Ag inside the microchannels acts as a seed layer for selective deposition of Cu. The Cu deposition is critical to device performance, as discussed later. As is evident in the optical image in Figure 3e and the SEM image in Figure 4d, the processed source and the drain electrodes have sharp edge definitions. Focused ion beam milling along the dotted line in Figure 4d reveals a thin coat of Cu/Ag metal on the sidewalls and bottom of the channel (Figure 4e).

In the second printing step, a semiconductor ink is delivered to the green reservoir (Figure 3b). We selected a p-type semiconducting polymer, poly(3-hexylthiophene) (P3HT). The P3HT ink wicks into the channel (w = 40 µm); capillary pressure drives the ink on top of the source and the drain electrodes before the flow bifurcates along the perimeter of the large rectangular cavity (Figure 3b,f). Note that bifurcation of capillary flow along the outlet reservoir walls, as opposed to flooding of the open space, is consistent with observations in microfluidic devices[22] and holds true for other inks as well, e.g., Ag ink (see Figure S3 in the Supporting Information). Evaporation of the ink solvent leaves behind a thin semiconducting polymer film between the source–drain electrodes. The film at the channel floor is remarkably smooth, as revealed by atomic force microscopy, with a root-mean-squared roughness over a 25 µm$^{[2]}$ area of only 2.1 ± 0.2 nm (see Figure S4 in the Supporting Information).

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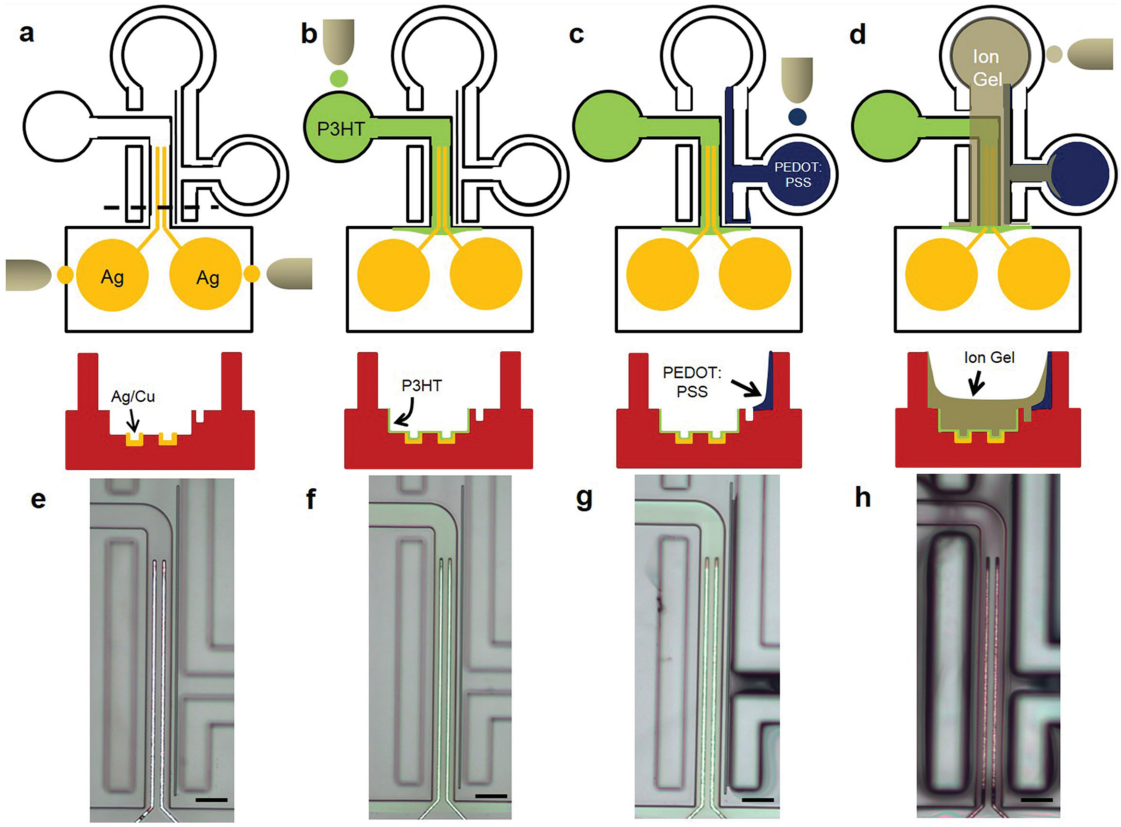

Figure 3. Fabrication of transistors using the SCALE process. Schematic of plan view of the device cavity (top) and cross section along the dotted line (below) after a) filling the source–drain cavities with Ag ink, followed by Cu electroless plating (not shown), b) filling the transistor channel with semiconductor ink (P3HT), c) patterning the gate electrode (PEDOT:PSS), and d) filling the device cavity with the dielectric ink (ion gel). Optical images of the imprinted device cavity on the plastic substrate surface after sequential patterning of e) Cu/Ag source–drain, f) P3HT semiconductor, g) PEDOT:PSS gate, and h) ion gel dielectric. Scale bar in (e–h) is 50 μm.

We employ a unique strategy for processing the gate electrode based on a commercially available inkjet-printable poly(3,4-ethylenedioxythiophene) polystyrene sulfonate (PEDOT:PSS) ink (0.8 wt% in H_2O). The PEDOT:PSS ink is dropped into the blue reservoir; the ink wicks into the channel and the liquid flow bifurcates at the channel outlet (Figure 3c). A narrow "stopper" channel (w = 3 μm), not connected to any reservoir, is strategically positioned between the P3HT channel and the PEDOT:PSS channel outlet (Figure 4c and f). During bifurcation of the PEDOT:PSS ink flow, the two leading edges of the capillary flow turn in opposite directions. The advancing contact line of the trailing bulk liquid is pinned to the top edge of the stopper and the ink does not trip over into the channel (Figure 3g and 4f). It has been shown that sharp microsteps on a substrate can pin an advancing contact line.[23,24] The pinning effect is highly reproducible and is also observed for the Ag ink (see Figure S6 in the Supporting Information). The stopper, therefore, not only facilitates precise patterning of the gate but also eliminates the possibility of shorting between the foot of the gate electrode and the P3HT film clung to the sidewall of its respective channel.

The final printing step involves loading the ion gel ink into the gray reservoir (Figure 3d). This reservoir is connected to a channel that encompasses all the other channels. The ion gel ink flows on top of all the underlying patterned channels; drying ensues and an ion gel film is left behind (Figure 3h). Note that the large height of the channel walls (≈46 μm) imparts sufficient momentum to the capillary flow such that it is uninterrupted by the discontinuity in one of the channel walls. Multiple shots of the ink are delivered for a sufficient buildup of gel thickness in the channel (Figure 4g). The completed device is annealed at 120 °C on a hot plate in an N_2-filled glovebox. An optical image of the completed EGT is shown in Figure 4b.

Figure 5a,b shows the transfer and output characteristics of an individual SCALE TFT, respectively. The transfer curve in Figure 5a was acquired with the gate voltage (V_G) swept from 0.5 to −0.9 V and back at 50 mV s^{-1} for drain voltage V_D = −0.8 V. The device turns on sharply near 0 V, with ON/OFF current ratio of ≈10^6, and negligible current hysteresis between the forward and the reverse scans. The output curve shows the expected modulation of the drain current (I_D) with gate voltage in both the linear and the saturation regimes, and the linear I_D–V_D relationship at low bias suggests nice Ohmic contacts despite the unusual electrode geometry. Devices processed with Ag-only source–drain contacts (i.e., without Cu) show much lower ON currents (see Figure S5 in the Supporting Information). A Cu overcoat on the Ag smooths the sharp channel edges, possibly facilitating a more conformal contact of the thin P3HT film

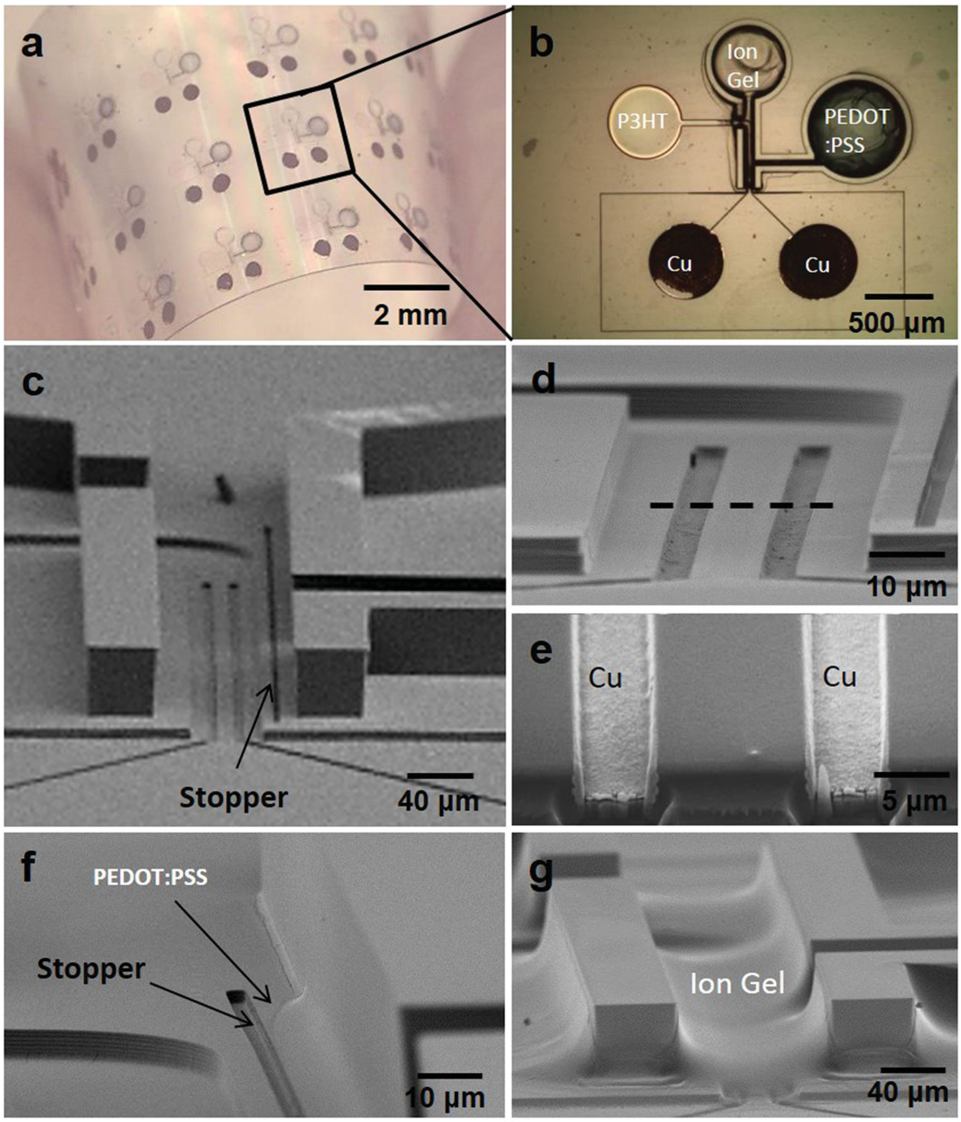

Figure 4. Optical and electron microscopy of printed transistors. Optical image of a) an array of printed transistors and b) a single device on an epoxy/PET substrate fabricated using the SCALE process. c) SEM image of the imprinted device cavity displaying all the channels employed in the fabrication process. d) SEM image of source–drain cavities filled with Ag/Cu metal after the printing and plating step. e) Focused ion beam cross section along the dotted line in (d), illustrating a thin coat of metal on the sidewalls and bottom of the channels. f) SEM image showing the printed PEDOT:PSS film pinned to the right edge of the stopper channel and g) printed ion gel film in the device cavity.

with the electrodes around the edges. We also employed Cu as a gate electrode for the EGTs by patterning the source, drain, and gate electrodes at the same time in the process flow. The devices showed similar performance metrics compared to the PEDOT:PSS-gated devices, although a slightly larger hysteresis was observed (see Figure S6 in the Supporting Information).

To quantify statistical variations in device performance, we printed 75 devices in five batches. A yield of ≈80% (59 out of 75 devices were functional) was observed. Device failure largely arose from errors in ink delivery to the reservoirs and/or impediment to capillary flow by dust particles on the substrate surface. As a first demonstration, these yields are acceptable—especially given that these devices are printed in air on a simple, laboratory benchtop using a single inkjet nozzle with manual x–y motion control. Figure 5c–e displays histograms of the statistical spread in key figures of merit for the 59 devices. The average saturation carrier mobility (μ) and the threshold voltage (V_{th}) are calculated to be 0.8 ± 0.4 cm^2 V^{-1} s^{-1} and –0.3 ± 0.0 V, respectively, from the plots of square root drain current ($I_D^{0.5}$) versus V_G, according to the standard saturation regime equation

$$I_D = \left(\frac{W}{2L}\right)\mu C_i (V_G - V_{th})^2$$

The channel width (W) and channel length (L) are 400 and 10 µm, respectively. The capacitance of the gel (C_i) is measured to be 5.2 µF cm^{-2} by capacitance–voltage characteristics (see

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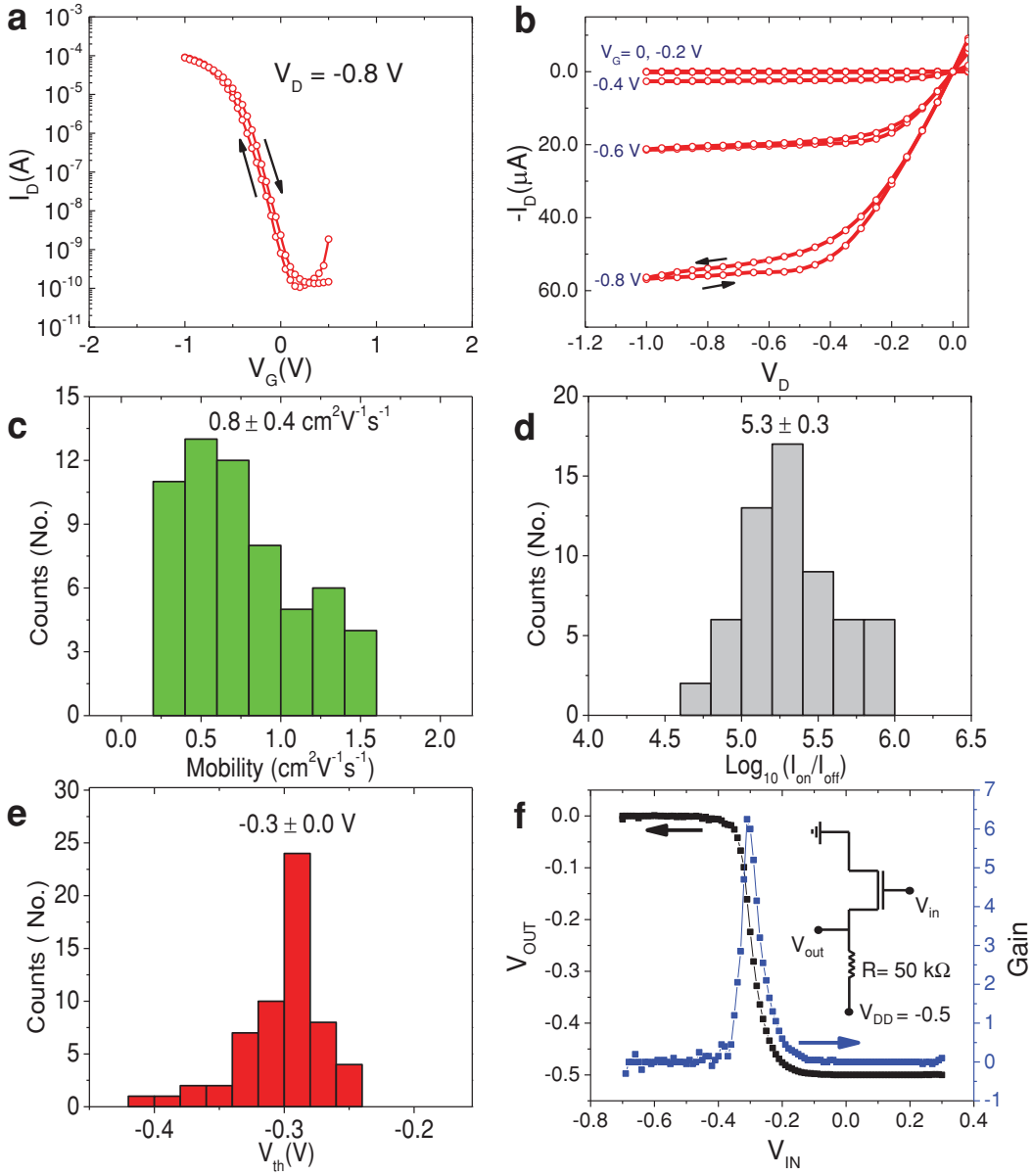

Figure 5. Electrical characterization of printed transistors and inverters. a) Transfer and b) output characteristics of printed P3HT EGTs (W/L = 400 μm/10 μm). Gate voltage sweep rate was 50 mV s^{-1}. c–e) Histograms of field effect mobility, I_{ON}/I_{OFF}, and threshold voltage of 59 printed devices, respectively. f) Quasistatic behavior of a resistor-loaded inverter with P3HT EGTs. The voltage gain (dV_{out}/dV_{in}) of the device was ≈6.2.

Figure S7 in the Supporting Information). The average $\log_{10}$ (I_{ON}/I_{OFF}) is an impressive 5.3 ± 0.3.

To demonstrate initial device integration with SCALE, we also fabricated simple resistor-loaded inverters by connecting P3HT EGTs in series with 50 kΩ resistors, both processed using methods described above. The circuit diagram and the input–output characteristics are presented in Figure 5f. The device shows good inverter action; the output voltage switches between –0.5 V (the applied drain voltage, V_{DD}) and 0 V as the input gate voltage is swept, and the voltage gain (dV_{out}/dV_{in}) is found to be ≈6.2.

For building complete electronic systems, strategies for fabricating interconnect crossovers are also essential. A crossover is essentially a metal–insulator–metal stack. We fabricated crossovers using the SCALE process by employing a three-tier imprint, a schematic of which is shown in **Figure 6**. First, Ag electrodes were fabricated by delivering Ag ink to the yellow reservoirs (Figure 6a). Next, a UV curable dielectric ink (NOA-73, Norland Products Inc.) dissolved in acetone (50:50 vol%) was printed into the two gray reservoirs (Figure 6b). Acetone was added to NOA 73 (a liquid prepolymer) as a viscosity modifier for inkjet printing. The ink flowed on top of the printed Ag channel, and then along the perimeter of the open cavity. The prepolymer was cured by irradiating the substrate with UV light, and the thick, cured film insulated the Ag electrode underneath. Fabrication was completed by simply delivering Ag ink to the

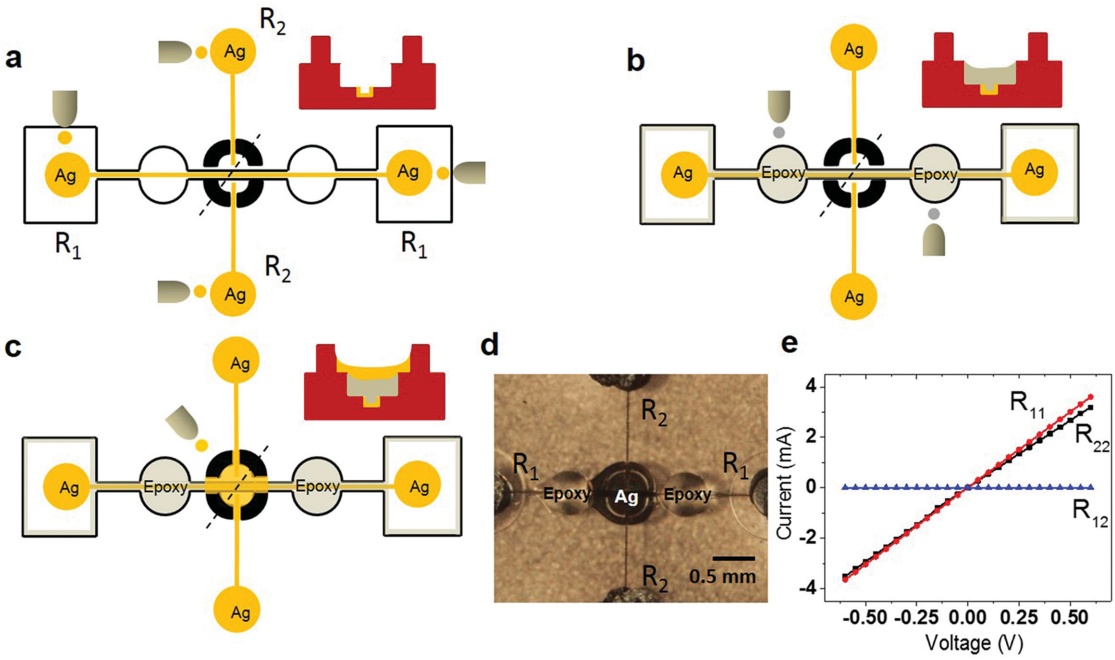

Figure 6. Fabrication of crossovers using the SCALE process and electrical characterization. Schematic of plan view of the device and cross section along the dotted lines after printing a) Ag ink in the yellow reservoirs, b) NOA epoxy ink in the gray reservoirs, and c) Ag ink again in the middle reservoir to connect the two Ag electrodes processed in step (a). d) Optical image of a completed device. e) Current–voltage characteristics of the printed device. Measurements across R_{11} and R_{22} yield linear *I*–*V* curves, but no current is observed across reservoirs R_1 and R_2 suggesting excellent insulation.

middle, top-tier reservoir (Figure 6c), thereby bridging the two Ag electrodes processed in the first step. An optical image of the completed device is shown in Figure 6d. *I*–*V* measurements across R_{11} and R_{22} yielded nice linear curves (Figure 6e) but no current was observed across R_{12} (Figure 6e, and Figure S8 in the Supporting Information), suggesting excellent insulation between the two perpendicular metal electrodes.

A potential drawback of the SCALE process is the large footprint of the devices; e.g., the substrate area per transistor in this work is 4 mm^2. This is primarily due to the large size of the reservoirs (≈0.5 mm diameter), necessitated by the limitations of our printing system. Future efforts will involve employing inkjet printheads capable of producing droplets with diameters 10 µm or smaller with automated *x*–*y* motion control. This will allow reduction in the reservoir size by a factor of 10 enabling an estimated integration density of 2000 devices cm^{-2}, an excellent figure of merit for printed electronics.

3. Conclusion

In summary, we have developed a novel self-aligned process, referred to as SCALE, for producing multilayered electronic devices on plastic substrates. Given the deformable nature of web substrates in continuous manufacturing systems, self-alignment of all the functional layers of electronic devices is of paramount importance. We have demonstrated that a wide variety of electronic devices including resistors, capacitors, transistors, and crossovers can be patterned using SCALE with excellent control over feature size, placement, and performance. The SCALE process essentially combines imprint lithography and inkjet printing, each of which can be implemented in R2R production formats.[25,26] By guiding inkjet-printed liquid drops into predefined device cavities on the substrate surface via capillarity, valuable materials are deposited precisely where they are required, thereby maintaining the benefits of additive manufacturing. Currently, patterns smaller than 100 nm can be achieved using imprint lithography, and therefore, devices much smaller than those presented in this work are accessible by SCALE. We anticipate that by employing state-of-the-art, low-volume (≈1 pL) inkjet printers and optimized liquid distribution capillary networks, unprecedented device integration densities on plastic are possible with SCALE, opening up new avenues for R2R printed electronics.

4. Experimental Section

Master Mold Fabrication: (i) Resistors and Capacitors: The master mold fabrication involved two photolithography cycles: Cycle (a)—A 4 in. silicon wafer (100) was prebaked at 200 °C for 5 min. Photoresist (NR71-1500P, Futurrex, Inc.) was spin-coated (300 rpm for 5 s followed by 3000 rpm for 45 s) on the silicon wafer, followed by softbake at 150 °C for 1 min. A predesigned mask was placed above the photoresist-coated silicon wafer and exposed to UV light for 28 s in an ultraviolet exposing system (Karl Suss MA6). The exposed wafer was baked at 110 °C for 1 min. The silicon wafer was immersed in the developer solution (RD6, Futurrex, Inc.) for 18 s, rinsed with DI water, and dried. The patterned silicon wafer was then dry-etched to 5 µm depth by reactive ion etching (SLR 770 Deep Trench Etcher). The etch rate was 0.9 µm min^{-1}. After etching, the photoresist is completely removed by sonicating the wafer in 1165 resist remover for 10 min. Cycle (b)—The wafer was cleaned by a Piranha solution (1:1 H_2SO_4 with H_2O_2) for 20 min at 120 °C and then rinsed with deionized (DI) water and dried. SU-8 2050 photoresist

(MicroChem Corp.) was spin-coated on the silicon wafer (500 rpm for 5 s followed by 3000 rpm for 30 s), followed by softbake at 65 °C for 3 min and 95 °C for 7 min. The photoresist-coated silicon wafer was exposed to UV light through a predesigned mask for 24 s. The exposed wafer was baked at 65 °C for 1 min and 95 °C for 7 min. The silicon wafer was immersed in the SU-8 developer solution for 5 min, rinsed with isopropanol alcohol, and dried. The height of the SU-8 features was about 46 μm. The completed wafer was hard-baked at 180 °C for 10 min.

(ii) Transistors: The master mold fabrication involved three parts: (a) All steps in cycle (a) from (i) were performed to create 6 μm deep reservoirs and channels in a silicon wafer. (b) Again, cycle (a) from (i) is repeated, but the spin-coating speed was 1800 rpm instead of 3000. The features were etched down to 3 μm. (c) All steps in cycle (b) from (i) were performed to obtain 46 μm high SU-8 features on the wafer surface. Optical images of the Si master mold have been shown in the Supporting Information in Figure S9.

(iii) Crossovers: The master mold fabrication involved three parts: (a) All steps in cycle (a) from (i) were performed to create 10 μm deep reservoirs and channels in a silicon wafer. (b) Again, cycle (a) from (i) is repeated, but the spin coating speed is kept 1800 rpm instead of 3000. The features were etched down to 5 μm. (c) All steps in cycle (b) from (i) were performed to obtain 46 μm high SU-8 features on the wafer surface.

Silanization: The patterened silicon master molds are silane-treated using the following procedure. The wafer was placed in a desiccator with 0.2 mL of trichloro(1*H*,1*H*,2*H*,2*H*-perfluorooctyl)silane (FOTS, Sigma-Aldrich) solution. The desiccator was then pumped down to 1 Torr of pressure to allow the FOTS solution to evaporate. The sample was left overnight for complete coverage.

PDMS Stamp Fabrication: For preparing the PDMS stamp, PDMS monomer and its curing agent (Dow Corning, Sylgard-184) were thoroughly mixed in a 10:1 weight ratio, respectively, and vacuum-degassed for 30 min. The Si master mold was placed in a plastic Petri dish, and 30 g of the PDMS prepolymer mixture was poured over the master mold and allowed to level out. The prepolymer mixture was then cured in an atmospheric oven at 60 °C for 12 h. After completely curing, the PDMS stamp was delaminated from the master mold. The stamp was then placed in an oven at 120 °C for 2 h.

Imprinted Flexible Substrate Fabrication: A flexible, UV-curable polymer, NOA-73 (Norland Products Inc.), was coated onto a 75 μm thick PET substrate. Prior to the coating, the PET substrate was air–plasma-treated for 3 min to promote the adhesion of the coating. The PDMS stamp was inserted into the liquid coating and pressed using a glass roller to drive out any entrapped air bubbles at the coating–stamp interface. The coating was cured by exposure to UV light for 20 min. Following complete cure, the stamp was delaminated, leaving behind imprinted features in the NOA/PET substrate.

Inks' Preparation: Reactive Ag ink was obtained from Electroninks, Inc., carbon black ink was purchased from Methode Electronics, Inc., P3HT was purchased from Rieke Metals, Inc., and the ink was prepared by dissolving the polymer in 1,2-dichlorobenzene (5 mg mL^{-1}). An inkjet printable version of PEDOT:PSS ink (0.8 wt% in H_2O) was purchased from Sigma-Aldrich. The ink was sonicated for 10 min just before printing. Ion gel ink was prepared by codissolving PS-PMMA-PS and [EMIM][TFSA] in *n*-butyl acetate in the following proportions: 2 wt% polymer, 8 wt% ionic liquid, and 90 wt% solvent. All the inks were filtered through 0.45 μm filter prior to printing.

Inkjet Printing: A custom-built drop-on-demand inkjet printer was employed, consisting of a MicroFab nozzle (MJ-AT-01), a charge-coupled device (CCD) camera, a strobe and strobe driver, a jetting driver, and a system computer, which controlled the pulse waveform. A reservoir filled with ink (1 mL) was attached to the nozzle. The nozzle was moved in the *x*–*y* direction manually using micrometers. A unipolar waveform for all the inks was employed consisting of rise time of 5 μs, fall time of 5 μs, and drive voltage of 100 V. The dwell times for the Ag, P3HT, PEDOT:PSS, and ion gel inks were 20, 25, 15, and 30 μs, respectively. All the inks were jetted at a frequency of 1 kHz. The nozzle's orifice diameter was 80 μm and diameters of a single ejected droplet for all the inks ranged between 60 and 70 μm. Prior to the printing, the substrate was air-plasma-treated for 3 min to enhance its surface-energy to augment capillary flow. All printing was performed in ambient atmosphere.

Cu Electroless Plating: The Cu electroless plating solution contained 2.704 g of $CuSO_4{\cdot}5H_2O$, 10.25 g of ethylenediaminetetraacetic acid disodium salt, 3.25 g of NaOH, 100 mL of DI water, and 25 mL of an aqueous solution of formaldehyde (37% by weight). The temperature of the bath was maintained at 55 °C. The printed substrate was kept in the bath for 3 min and taken out, rinsed with DI water, and dried using an air gun.

Electrical Characterization of Devices: The capacitance measurements were performed using an HP4192A LF impedance analyzer. Current–voltage characteristics for resistors and conductors were measured using two Keithley 236 source measurement units. Transistor current–voltage characteristics were measured using two Keithley 236 source measurement units and a Keithley 6517 electrometer. All measurements were performed in N_2 atmosphere.

Supporting Information

Supporting Information is available from the Wiley Online Library or from the author.

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